IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl.No.:	10/717,235	Confirmation No.: 6910
Appellant:	Kubota	
Filed:	11/18/2003	
TC/AU:	2629	
Examiner:	Sheng, Tom V.	
Docket:	TI-35414	
Cust.No.:	23494	

APPEAL BRIEF

Commissioner for Patents
P.O.Box 1450
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Sir:

The attached sheets contain the Rule 41.37 items of appellant's Appeal Brief pursuant to the Notice of Appeal filed 03/04/2007. The Director is hereby authorized to charge the fee for filing a brief in support of the appeal plus any other necessary fees to the deposit account of Texas Instruments Incorporated, account No. 20-0668.

Respectfully submitted,

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Rule 41.37(c)(1)(i) Real party of interest

Texas Instruments Incorporated owns the application.

Rule 41.37(c)(1)(ii) Related appeals and interferences

There are no related dispositive appeals or interferences.

Rule 41.37(c)(1)(iii) Status of claims

Pursuant to MPEP 1205.02, for each claim in the case appellant states the status as follows:

Claim 1: rejected

Claim 2: objected to

Claim 3: objected to

Claim 4: objected to

Claim 5: rejected

Claim 6: rejected

Claim 7: rejected

Claim 8: rejected

Claim 9: rejected

Claim 10: rejected

Claim 11: objected to

Claim 12: rejected

Claim 13: rejected

Pursuant to MPEP 1205.02, appellant identifies each claim on appeal as follows

Claim 1: on appeal

Claim 5: on appeal

Claim 6: on appeal

Claim 7: on appeal

Claim 8: on appeal

Claim 9: on appeal

Claim 10: on appeal

Claim 12: on appeal

Claim 13: on appeal

Rule 41.37(c)(1)(iv) Status of amendments

There is no amendment after final rejection.

Rule 41.37(c)(1)(v) Summary of claimed subject matter

The independent claims on appeal consist of circuit claim 1 and circuit claim 8.

The subject matter of claim 1 is an integrated circuit for scan driving being used in sequentially selecting and driving scanning lines in a display, which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration, and which has a pixel arranged at each cross point; in this integrated circuit for scan driving, comprising:

a chip, having plural output pads arranged as a column in a first direction (application page 17, line 20 to page 18, line 8; FIG.1, OUT1, OUT2, ..., OUT176), plural drive circuits for driving said scanning lines to the active state through said output pads (application page 17, line 20 to page 18, line 3; FIG.1, DR1, DR2, ...DR176), respectively, and plural selection circuits for individually selecting said driver circuits (application page 17, line 20 to page 18, line 8; FIG.1, SREG1, SREG2, ... SREG176) in a line-sequential scanning cycle in an order corresponding to the order of said scanning lines (application page 17, line 22, page 18, lines 3-4; FIG.1);

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region (application page 17, lines 20-27; FIG.1, A_{ODD}),

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second region adjacent to said first region in said first direction (application page 18, lines 1-8; FIG.1, A_{EVEN});

said first region, in an order corresponding to the order of said odd-numbered scanning lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, (application page 17, lines 20-23; FIG.1, OUT1, OUT3, ..., DR1, DR3, ..., SREG1 SREG3 ...) and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines are arranged in the same row in the second direction nearly orthogonal to said first direction (application page 17, lines 23-26; FIG.1, OUTi-DRi-SREGi);

and, in said second region, in an order corresponding to the order of said even-numbered scanning lines, said even-numbered output pads, driver circuits and selection circuits are arranged as columns in said first direction (application page 18, lines 1-4; FIG.1, OUT2, OUT4, ..., DR2, DR4, ..., SREG2, SREG4, ...), and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines being arranged in the same row in said second direction (application page 18, lines 4-7; FIG.1, OUTi-DRi-SREGi).

The subject matter of claim 8 is a type of integrated circuit for scan driving for sequentially supplying scan drive signal to the scanning electrodes of a display device; comprising:

a first shift register (application page 17, lines 25-26; FIGS.1-2, SR_O), which has plural register circuits connected in series (application page 17, lines 25-26; FIG.2, SREG1, SREG3, ...), and which sequentially transfers the first shift data corresponding to a first clock signal (application page 18, line 26 to page 19, line 1; page 19, lines 6-7; page 18, lines 14-17; FIG.4, 2CLK_O),

a first drive section, which has plural driver circuits (application page 17, lines 20-21; FIG.2, DR1, DR3, ...) corresponding to the plural register circuits of said first shift register, respectively (application page 17, lines 24-25; FIG.2, SREG1-DR1, SREG3-DR3, ...), and which has said plural driver circuits output drive signals corresponding to said first shift data outputs from the plural register circuits of said first shift register, respectively (application page 22, lines 3-7;

page 23, lines 3-16; page 24, lines 23-26; page 25, lines 1-4; FIG.2, OUTBUF1, OUTBUF3, ...; FIG.4, SREG1OUT, SREG3OUT, ..),

a second shift register (application page 18, lines 7-8; page 19, lines 7-8; FIGS.1-2, SR_E), which has plural register circuits connected in series (application page 18, lines 7-8; FIG.2, SREG2, SREG4, ...), and which sequentially transfers the second shift data shifted in phase by half a period of a second clock signal with respect to said first shift data corresponding to the second clock signal with its phase deviated by 180° from said first clock signal (application page page 19, lines 1-5; page 19, lines 7-9; page 18, lines 17-19; FIG.4, 2CLK_E),

and a second drive section, which has plural driver circuits (application page 18, lines 1-2; FIG.2, DR2, DR4, ...) corresponding to the plural register circuits of said second shift register, respectively (application page 18, lines 2-7; FIG.2, SREG2-DR2, SREG4-DR4, .), and which has said plural driver circuits output drive signals corresponding to said second shift data output outputs from the plural register circuits of said second shift register, respectively (application page 22, lines 22-25; page 23, line 23 to page 24, line 4; page 24, lines 13-17 and 26-29; page 25, lines 1-4; FIG.2, OUTBUF2, OUTBUF4, ...; FIG.4, SREG2OUT, SREG4OUT, ..);

said drive signals are output alternately from the various driver circuits of said first drive section and the various driver circuits of said second drive section, corresponding to said first or second shift data (application page 21, line 15 to page 22, line 21, et seq.; FIG.4, SREG1OUT, SREG2OUT, SREG3OUT, ...).

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Rule 41.37(c)(1)(vi) Grounds of rejection to be reviewed on appeal

The grounds of rejection to be reviewed on appeal are:

1. Claim 1 was rejected under 35 USC § 112, ¶ 2 as indefinite.

2. Claims 1 and 5-7 were rejected under 35 USC § 103(a) as being unpatentable over admitted prior art in view of Fujikawa (USP 6,545,655).

3. Claims 8-10 and 12-13 were rejected under 35 USC § 103(a) as being unpatentable over admitted prior art in view of Fujikawa (USP 6,545,655) and further in view of Wakai et al. (USP 4,908,710).

Rule 41.37(c)(1)(vii) Arguments

1. Claim 1 was rejected as indefinite due to lack of antecedent basis for "the second direction" in lines 20-21.

Claim 1: Claim 1, lines 20-21 contain the first instance of "second direction" as follows: "... in the same row in the second direction nearly orthogonal to said first direction; ...". Thus the second direction is already defined by orthogonality to the first direction, and thus use of definite article "the" with "second direction" is permissible. Further, claim 1 uses "said" for references, so "the" does not have to be a reference.

2. Claims 1 and 5-7 were rejected as unpatentable over admitted prior art in view of Fujikawa.

Claims 1 and 5-7: The Examiner cited application prior art Figs.9-10 for the items of claim 1 except for the arrangement of SREG1-SREG176 with respect to drivers DR1-DR176, and added Fujikawa Fig.6 for v-drivers 25-26 corresponding to even and odd scanning rows and criss-crossed connections to the LCD panel. However, Fujikawa does not show the internal arrangement of the items within v-drivers 25,26 which relate to the claim 1 requirements. That is, Fujikawa shows arrangements of regions of pixels with drivers, but does not show any pertinent internal arrangements of items within the drivers. Thus the admitted prior art plus Fujikawa do not make base claim 1 obvious.

3. Claims 8-10 and 12-13 were rejected as unpatentable over admitted prior art in view of Fujikawa and Wakai.

Claims 8-10 and 12-13: The Examiner applied admitted prior art and Fujikawa as in the claim 1 rejection plus added Wakai which shows shift register clocks ϕyo and ϕye. However, Wakai has shift registers 401, 402 of Fig.4 with

clocks ϕyo and ϕye on opposite sides of the LCD panel; thus Wakai would not make obvious anything about two shift registers and drivers on the same side. Consequently, the claims are patentable over the references.

Rule 41.37(c)(1)(viii) Claims appendix

Claim 1: An integrated circuit for scan driving being used in sequentially selecting and driving scanning lines in a display, which has said plural scanning lines and plural signal lines arranged crossing each other in a matrix configuration, and which has a pixel arranged at each cross point; in this integrated circuit for scan driving, comprising:

a chip, having plural output pads arranged as a column in a first direction, plural drive circuits for driving said scanning lines to the active state through said output pads, respectively, and plural selection circuits for individually selecting said driver circuits in a line-sequential scanning cycle in an order corresponding to the order of said scanning lines;

the odd-numbered output pads, driver circuits and selection circuits corresponding to odd-numbered scanning lines are all arranged in a first region,

the even-numbered output pads, driver circuits and selection circuits corresponding to the even-numbered scanning lines being all arranged in a second region adjacent to said first region in said first direction;

said first region, in an order corresponding to the order of said odd-numbered scanning lines, said odd-numbered output pads, driver circuits and selection circuits being arranged as columns in said first direction, respectively, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines are arranged in the same row in the second direction nearly orthogonal to said first direction;

and, in said second region, in an order corresponding to the order of said even-numbered scanning lines, said even-numbered output pads, driver circuits and selection circuits are arranged as columns in said first direction, and, at the same time, said output pads, driver circuits and selection circuits corresponding to each of the scanning lines being arranged in the same row in said second direction.

Claim 2: The integrated circuit for scan driving as in Claim 1 comprising:

said odd-numbered selection circuits are made of individual flip-flops that overall form the first shift register; the first shift data provided by the frame period is transferred sequentially to the latter-stage flip-flops in synchronization with the first transfer clock signal at a frequency half that of the line-sequential scanning cycle; by means of the output signals of the flip-flops with said first shift data latched in them, the corresponding driver circuits are selected;

said even-numbered selection circuits are made of individual flip-flops that overall form the second shift register; the second shift data provided by frame period is transferred sequentially to the latter-stage flip-flops in synchronization with the second transfer clock signal at a frequency half that of the line-sequential scanning cycle and in a phase opposite to that of said first transfer clock signal; and, by means of the output signals of the flip-flops with said second shift data latched in them, the corresponding driver circuits are selected.

Claim 3: The integrated circuit for scan driving as in Claim 2 wherein said first and second shift registers allow bidirectional transfer of, respectively, said first and second shift data.

Claim 4: The integrated circuit for scan driving as in Claim 1 wherein said integrator integrated circuit includes:

a transfer clock generator that divides the fundamental clock signal that defines the cycle of line-sequential scanning in half,

and a shift data generator that generates said first and second shift data in two consecutive cycles of said fundamental clock signal corresponding to the start pulse that indicates the timing of the start of a frame.

Claim 5: The integrated circuit for scan driving as in Claim 1 wherein said first direction corresponds to the longitudinal direction of said chip, and said output pads are arranged as a column along one edge extending in the longitudinal direction of said chip.

Claim 6: The integrated circuit for scan driving described in Claim 5 wherein the input pads for input of the desired power source voltage or signal are arranged as a column along the other edge in the longitudinal direction of said chip.

Claim 7: The integrated circuit for scan driving as in Claim 3 wherein said chip is assembled by means of TCP.

Claim 8: A type of integrated circuit for scan driving for sequentially supplying scan drive signal to the scanning electrodes of a display device; comprising:

a first shift register, which has plural register circuits connected in series, and which sequentially transfers the first shift data corresponding to a first clock signal,

a first drive section, which has plural driver circuits corresponding to the plural register circuits of said first shift register, respectively, and which has said plural driver circuits output drive signals corresponding to said first shift data outputs from the plural register circuits of said first shift register, respectively,

a second shift register, which has plural register circuits connected in series, and which sequentially transfers the second shift data shifted in phase by half a period of a second clock signal with respect to said first shift data corresponding to the second clock signal with its phase deviated by 180° from said first clock signal,

and a second drive section, which has plural driver circuits corresponding to the plural register circuits of said second shift register, respectively, and which has said plural driver circuits output drive signals corresponding to said second shift data output outputs from the plural register circuits of said second shift register, respectively;

said drive signals are output alternately from the various driver circuits of said first drive section and the various driver circuits of said second drive section, corresponding to said first or second shift data.

Claim 9: The integrated circuit for scan driving as in Claim 8 wherein the register circuits of said first shift register and the driver circuits of said first drive section are arranged in order of activation along the a first direction; and the register circuits of said second shift register and the driver circuits of said second drive section are arranged in order of activation along said first direction.

Claim 10: The integrated circuit for scan driving as in Claim 9 wherein said first and second shift registers are bidirectional shift registers that allow transfer of shift data bidirectionally; said first shift data is supplied to the register circuit in the initial stage or the register circuit in the final stage of said first shift register, and said second shift data is supplied to the register circuit of the initial stage or the register circuit of the final stage of said second shift register.

Claim 11: The integrated circuit for scan driving as in Claim 8 wherein said integrated circuit has a signal generator, to which the reference clock signal having a frequency double that of said first and second clock signals as well as a start pulse are input, and which generates said first and second clock signals and said first and second shift data on the base of said reference clock signal and said start pulse.

Claim 12: The integrated circuit for scan driving as in Claim 9 wherein said first and second shift registers and said first and second drive sections are formed on

a rectangular semiconductor chip, and said first direction is the longitudinal direction of said semiconductor chip.

Claim 13: The integrated circuit for scan driving described in Claim 12 wherein the odd-numbered drive signals are sequentially output from the various driver circuits of said first drive section, and the even-numbered drive signals are sequentially output from the driver circuits of said second drive section.

Rule 41.37(c)(1)(ix) Evidence appendix

none

Rule 41.37(c)(1)(x) Related proceedings appendix

none